IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTORS: Hideshi ABE

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SERIAL NO.: Not yet assigned

FILED: June 11, 2001 EXAMINER: F. ABRAHAM

GROUP ART UNIT: 2826

PARENT SERIAL NO.: 08/965,980

TITLE: **SEMICONDUCTOR APPARATUS, MANUFACTURING METHOD THEREFOR, SOLID STATE IMAGING DEVICE AND MANUFACTURING METHOD THEREFOR**

PRELIMINARY AMENDMENT "A" TO 1.53(b) DIVISIONAL

BOX Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

S I R:

Regarding the 37 CFR 1.53(b) Divisional filed on June 11, 2001, please enter the following amendments and consider the remarks below.

IN THE SPECIFICATION

On page 1, between lines 1 and 2, please add the following paragraph:

--RELATED APPLICATION DATA

This patent is a divisional application of serial number 08/965,980, filed on November 7, 1997. This patent application claims priority to Japanese Application No. P8-296938, filed November 8, 1996, which application is incorporated herein by reference to the extent permitted by law.--.

IN THE CLAIMS

Please cancel claims 1-13 and add 14-17 as follows:

14. A method of manufacturing a semiconductor apparatus comprising the steps of:

forming a bypass film from an insulation film through which a leak current is able to easily flow as compared with a gate insulation film of a MIS transistor and forming a gate electrode which extends above said bypass film; and

performing a work process directed to the manufacture of the semiconductor apparatus while performing destaticization through said bypass film.

15. A method of manufacturing a semiconductor apparatus according to claim 14, further comprising the steps of:

selectively etching a gate insulation film of a region forming said bypass film to make the same thin after said gate insulation film of said MIS transistor has been formed; and

forming said gate electrode to have a pattern extending from a region of said MIS transistor to a portion above said bypass film.

16. A method of manufacturing a semiconductor apparatus according to claim 14, further comprising the steps of:

forming a first gate insulation film of said MIS transistor, then selectively etching off said first gate insulation film at a region of said bypass film and forming a second gate insulation film which will become said bypass film; and

then forming said gate electrode to have a pattern extending from a region of said MIS transistor to a portion above said bypass film.

17. A method of manufacturing a solid state image device comprising the steps of:

forming a bypass film through which a leak current is able to easily flow as compared with a gate insulation film, between a wiring for connecting each gate electrodes of a MOS transistor forming the pixel and a drain region, and

carrying out a work process while performing destaticization through said bypass film.

REMARKS

This amendment is filed to claim priority to the parent and Japanese priority application and to incorporate same by reference. Also, the subject matters of claims 9-11 and 13 have been recast as claims 14-17, respectively.

Respectfully submitted,
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service in an envelope addressed to: BOX Patent Application, Assistant Commissioner for Patents, Washington, D.C. 20231 on June 11, 2001.

Rose M. Garza Date: June 11, 2001